Please amend the Claims as follows:

Claim 1 (Currently Amended):

1. For use in an instruction processor that executes instructions included in a predetermined instruction set at an execution rate determined by a system clock signal, a synchronous instruction pipeline, comprising:

a pipeline execution circuit to process a first predetermined number of instructions simultaneously, each of said first predetermined number of instructions being in a respectively different stage of execution within said pipeline execution circuit, instructions being capable of advancing to a next stage of execution within said pipeline execution circuit at a time determined by the system clock signal; and

a pipeline fetch circuit coupled ~~directly~~ to provide each of the first predetermined number of instructions directly to said pipeline execution circuit, the pipeline fetch circuit to retain a second predetermined number of instructions simultaneously, each of said second predetermined number of instructions being in a respectively different stage of processing within said pipeline fetch circuit, an instruction being capable of advancing to a next stage of execution within said pipeline fetch circuit at a time determined by the system clock signal and independently of the times at which instructions advance to a next stage of execution within said pipeline execution circuit.

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Claim 2: (Original) The synchronous instruction pipeline of Claim 1, wherein said pipeline fetch circuit includes an instruction queue to store a predetermined maximum number of the instructions that are each ready to be processed by said pipeline fetch circuit.

Claim 3: (Original) The synchronous instruction pipeline of Claim 1, wherein said pipeline fetch circuit includes a pre-decode logic circuit to generate pre-

decode signals for an instruction that is in a pre-decode stage of processing within said pipeline fetch circuit, and wherein an instruction can enter said pre-decode stage of processing independently of the movement of instructions through said pipeline execution circuit.

Claim 4: (Original) The synchronous instruction pipeline of Claim 3, wherein said pipeline fetch circuit includes a decode logic circuit coupled to said pre-decode logic circuit to generate decode signals for an instruction that is in a decode stage of processing within said pipeline fetch circuit, and wherein an instruction can enter said decode stage of processing from said pre-decode stage of processing independently of the movement of instructions through said pipeline execution circuit.

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Claim 5: (Original) The synchronous instruction pipeline of Claim 4, wherein said pipeline fetch circuit includes a first selection circuit coupled to said pre-decode logic circuit to allow an instruction to be received by said pre-decode logic circuit at a time determined by the system clock signal if said decode logic circuit is available to accept an instruction currently being executed by said pre-decode logic circuit.

Claim 6: The synchronous instruction pipeline of Claim 5, wherein said pipeline fetch circuit includes a second selection circuit coupled to said decode logic circuit to allow an instruction to enter said decode stage of execution at a time determined by the system clock signal if said decode logic circuit is not processing another instruction.

Claim 7 (Previously Amended):

7. The synchronous instruction pipeline of Claim 5, wherein said pipeline execution circuit includes a microcode-controlled sequencer to control execution

of extended stages of execution of extended-mode ones of the instructions, wherein during said extended stages of execution, ones of the instructions being executed by said pipeline execution circuit are not advancing to a next stage of execution within said pipeline execution circuit, and wherein said first selection circuit includes a control circuit to allow an instruction to enter said pre-decode stage of processing while said extended-mode ones of the instructions are not advancing to a next stage of execution within said pipeline execution circuit.

Claims 8-20 (Canceled)

Please add the following new Claims:

Claim 21 (New)

21. For use in an instruction processor, a synchronous pipeline circuit, comprising:

an execution circuit to provide a first predetermined number of execution stages, each being capable of performing a respective processing operation on a respective instruction; and

a fetch circuit coupled to the execution circuit to provide a second predetermined number of fetch stages, each fetch stage being capable of performing a respective pre-execution operation on a respective instruction, the fetch circuit to transfer each instruction processed by the fetch circuit directly from one of the fetch stages to one of the execution stages, ones of the instructions processed within the fetch stages being capable of advancing to different available fetch stages independently of whether instructions are advancing within the execution stages.

Claim 22 (New)

22. The pipeline circuit of Claim 21, wherein one of the fetch stages includes instruction address generate logic to predict which instructions are to enter the fetch stages.

Claim 23 (New)

23. The pipeline circuit of Claim 22, wherein the instruction address generate logic includes a circuit to clear ones of the fetch stages in response to a determination that instruction execution was re-directed.

Claim 24 (New)

24. The pipeline circuit of Claim 21, and further including

a memory to store instructions;

a queue coupled to the memory to temporarily store at least one instruction fetched from the memory; and

a circuit coupled to the queue and to at least one of the fetch stages to fetch an instruction from the queue for presentation to at least one of the fetch stages.

Claim 25 (New)

25. The pipeline circuit of Claim 24, wherein the circuit coupled to the queue is capable of retrieving instructions from the queue for presentation to the at least one of the fetch stages regardless of whether instructions are advancing within the execution stages.

Claim 26 (New)

26. The pipeline circuit of Claim 21, wherein at least one of the execution stages includes a microcode-controlled sequencer to control execution of extended-mode instructions, and wherein during some stages of execution of the

extended-mode instructions, instructions are not advancing within the execution circuit.

Claim 27 (New)

27. A synchronous instruction pipeline circuit for processing instructions within a data processing system, comprising:

a first predetermined number of fetch stages to simultaneously process at least a first predetermined number of instructions;

a second predetermined number of execution stages to simultaneous process a second predetermined number of instructions, each received directly from one of the fetch stages; and

wherein at least one of the fetch stages is capable of providing an instruction to a different one of the fetch stages that is ready to receive an instruction irrespective of movement of instructions between the execution stages.

Claim 28 (New)

28. The pipeline circuit of Claim 27, wherein one of the fetch stages includes address generate logic to predict which instructions are to enter the fetch stages for processing.

Claim 29 (New)

29. The pipeline circuit of Claim 28, wherein the address generate logic includes a circuit to flush one or more instructions from the fetch stages if it is determined that a misprediction occurred.

Claim 30 (New)

30. The pipeline circuit of Claim 27, and further including:

a memory; and

a storage device coupled to one of the fetch stages and to the memory to store instructions retrieved from the memory, wherein a predetermined number of instructions may be stored within the storage device regardless of whether instructions are advancing within the fetch stages.

Claim 31 (New)

31. The pipeline circuit of Claim 27, wherein one of the execution stages includes a microcode sequencer to execute predetermined ones of the instructions in a manner that may temporarily affect movement of instructions within the execution stages.

Claim 32 (New)

32. A synchronous instruction pipeline to execute instructions, comprising:

an execution circuit having a first predetermined number of execution stages to execute a first predetermined number of instructions substantially simultaneously; and

a fetch circuit having a second predetermined number of fetch stages to perform pre-execution operations on at least a second predetermined number of instructions substantially simultaneously, one of the fetch stages being coupled to provide each instruction processed by the fetch circuit directly to one of the execution stages, at least one of the at least second predetermined number of instructions being capable of advancing between different ones of the fetch stages regardless of whether an instruction is being transferred by the fetch circuit to the execution circuit.

Claim 33 (New)

33. The pipeline of Claim 32, wherein the fetch circuit includes an instruction address generate section to determine which instructions are to enter the fetch circuit.

Claim 34 (New)

34. The pipeline of Claim 33, wherein the instruction address generate section includes a circuit to remove instructions from the fetch circuit during a pipeline flush operation.

Claim 35 (New)

35. The pipeline of Claim 32, and further including:

a memory to store instructions; and

a queue coupled to store instructions from the memory, the queue further being coupled to provide an instruction to the fetch circuit if one of the fetch stages is available and irrespective of whether an instruction is being provided from the fetch circuit to the execution circuit.

Claim 36 (New)

36. The pipeline of Claim 35, and further including a circuit coupled to the queue to allow an instruction to be stored to the queue independently of whether an instruction is advancing within the fetch circuit.

Claim 37 (New)

37. The pipeline of Claim 36, wherein the circuit allows a predetermined maximum number of instructions to be stored to the queue independently of whether an instruction is advancing within the fetch circuit.

Claim 38 (New)

38. The pipeline of Claim 37, wherein the one of the fetch stages includes a circuit to allow retrieval of an instruction from either the memory or from the queue.

Claim 39 (New)

39. The pipeline of Claim 32, wherein the fetch circuit includes a circuit that allows instructions to advance within the second predetermined number of fetch stages if one of the execution stages is performing a predetermined function.

Claim 40 (New)

40. A method of processing instructions within a synchronous pipeline of an instruction processor, comprising:

a.) performing pre-execution operations on a first predetermined number of instructions substantially simultaneously within a first predetermined number of fetch stages of the pipeline;

b.) executing a second predetermined number of instructions substantially simultaneously within a second predetermined number of execution stages of the pipeline, wherein each of the second predetermined number of instructions were received directly from one of the fetch stages; and

c.) allowing one or more of the first predetermined number of instructions to advance between ones of the fetch stages independently of whether any of the second predetermined number of instructions are advancing between ones of the execution stages.

Claim 41 (New)

41. The method of Claim 40, and further including:

fetching an instruction from a memory;

storing the instruction within a queue; and

retrieving the instruction from the queue to undergo a pre-execution operation within a predetermined one of the fetch stages.

Claim 42 (New)

42. The method of Claim 41, wherein at least one of the storing and the retrieving step is performed independently of whether instructions are advancing between ones of the execution stages.

Claim 43 (New)

43. The method of Claim 42, wherein ones of the steps are repeated for multiple instructions.

Claim 44 (New)

44. The method of Claim 40, wherein one of the execution stages includes a microcode-controlled sequencer for executing extended-mode instructions, and further including executing one of the extended-mode instructions in a manner that temporarily delays the advancing of instructions between ones of the execution stages.

Claim 45 (New)

45. The method of Claim 40, and further including:

providing an indication that one or more predetermined operations are occurring within one or more of the execution stages; and

in response to the indication, allowing instructions to advance within the fetch stages.

Claim 46 (New)

46. A pipeline circuit for use in an instruction processor, comprising:

instruction fetch means for performing pre-execution operations on a first predetermined number of instructions substantially simultaneously within a first predetermined number of fetch stages;

instruction execution means for executing a second predetermined number of instructions substantially simultaneously within a second

predetermined number of execution stages, each of the second predetermined number of instructions being received directly from one of the fetch stages; and wherein

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the instruction fetch means includes means for allowing at least one of the first predetermined number of instructions to advance within the fetch stages irrespective of whether instructions are advancing within the execution stages.